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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,016	02/03/2004	CHIEN-SHENG YANG	12030-US-PA	2015

31561 7590 01/12/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,016	YANG, CHIEN-SHENG	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-9 and 12* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,9 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 27 September 2005 have been fully considered but they are not persuasive.

The applicant has amended claim 1 to recite that a capacitor electrode, between the substrate and the pixel electrode, does not cover the data line and the scan line. The claim already recites an electrical field shielding layer which is between the data line and the pixel electrode. The applicant argues that the references cited in the previous office action show their capacitor electrodes overlapping the data and scan lines.

This raises problems of new matter and claim interpretation. First, it is not clear to the examiner where support for this amendment is found in the original specification. If the figures are the sole source of support, then the support is lacking, since there is not a plane-view showing this feature and the cross-sections are ambiguous as to whether the data and scan lines are covered by the capacitor electrode. Is there clear support for the amendment that the examiner has overlooked? Second, as shown in Fig. 2E, the electrical field shielding (EFS) layer [245] and the capacitor electrode [240a] are made at the same time of the same material; the specification states that the EFS layer also stores charge with the pixel electrode, so the EFS layer is itself a capacitor electrode. The specification does not appear to state whether or not they are integral, separate but electrically connected to each other, or isolated from each other. If they

were integral, then the EFS layer and the capacitor electrode would not be clearly distinguishable from each other and the limitation that the capacitor electrode does not cover the data and scan lines would be even more problematic since the EFS layer clearly overlaps at least part of the data and scan lines. Is there anything in the original filing which would make it clear how to distinguish the EFS layer from the capacitor electrode, or what these layers would cover in plane-view? Third, even if they can be distinguished in the present specification, the scope of the claims is now unclear due to the ambiguity in defining the EFS layer and capacitor electrode. It seems reasonable in interpreting the prior art references to describe a section of a capacitor electrode which does not cover the scan and data lines as the "capacitor electrode", while another section (which can cover at least a part of the data/scan lines) between the data line and the pixel electrode is the "EFS layer" of the claim. This is the basis for the prior art rejections below.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-3, 6, 7, 9, and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As discussed above, the examiner does not see where the original filing has support for the amended claim limitation that the capacitor electrode does not cover the data line and the scan line.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-3, 6, 7, 9, and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As discussed above, the terms electrical field shielding (EFS) layer and capacitor electrode appear to the examiner to be ambiguous, since the EFS layer itself acts as a capacitor layer. Where does one begin and the other end? Even if they are isolated from each other in the present specification (which is not clear to the examiner), how are they to be distinguished from each other in other devices? This question is now important as the amended claim limitation recites that the capacitor electrode does not cover the data and scan lines, but leaves open the possibility that the EFS layer does. For examining purposes, it is assumed that a section of a capacitor electrode which does not cover the scan and data lines can be the "capacitor electrode", while another section (which can cover at least a part of the data/scan lines) between the data line and the pixel electrode can be the "EFS layer" of the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by *Matsushima,* U.S. Patent No. 5,917,563.

Matsushima discloses [see Figs. 2 and 4, for instance] a pixel structure, adapted to be disposed on a substrate [10], comprising a scan line [16], a data line [20], an active element, disposed near an intersection of the scan and data line, electrically coupled to the scan and data line; a capacitor electrode [a part of 26a not covering the scan and data lines]; a pixel electrode [25] disposed over the substrate and capacitor electrode and electrically coupled to the active element, wherein the pixel electrode and the capacitor electrode form a pixel storage capacitor; and an electrical field shielding layer [a part of 26a between the data line and the pixel electrode] disposed between the data line and the pixel electrode, where the capacitor electrode, between the substrate and the pixel electrode, does not cover the data and scan lines. Claim 1 is therefore anticipated.

8. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by *Zhang et al.,* U.S. Patent No. 6,115,088.

Zhang discloses [see Fig. 10, for instance] a pixel structure, adapted to be disposed on a substrate, comprising a scan line [104], a data line [105], an active element, disposed near an intersection of the scan and data line, electrically coupled to the scan and data line; a capacitor electrode [a part of 106 not covering the scan and data lines]; a pixel electrode [107] disposed over the capacitor electrode and electrically coupled to the active element, wherein the pixel electrode and the capacitor electrode form a pixel storage capacitor; and an electrical field shielding layer [a part of 106 between the data line and the pixel electrode] disposed between the data line and the pixel electrode. Claim 1 is therefore anticipated.

Zhang also discloses that the capacitor electrode, and the electrical field shielding layer, and the pixel electrode are made from ITO [col. 3, lines 31-48], so claim 12 is also anticipated.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Matsushima,* U.S. Patent No. 5,917,563 as applied above, in view of *Takahara et al.,* U.S. Patent No. 5,673,127.

Matsushima discloses the active element comprising a polysilicon [11] thin film transistor, but not necessarily that it is a low temperature polysilicon TFT. *Takahara* discloses using a low-temperature polysilicon TFT, and teaches that it is preferred (over high-T polysilicon) because "a drive circuit can be built in and the display panel can be made at a low price" [col. 19, lines 48-55]. It would have been obvious to one of ordinary skill in the art at the time of the invention to do so in the device of *Matsushima*, motivated by this teaching. Claim 2 is therefore unpatentable.

Matsushima discloses a drain/source conductive layer [20a, 21a, etc.] wherein the active element is electrically coupled to the data line and the pixel electrode through the drain/source conductive layer, so claim 3 is also unpatentable.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Schechter
Primary Examiner
Technology Center 2800
6 January 2006